Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A data processing system for qualifying events when an interrupt occurs, comprising:

a performance monitoring unit;

one or more hardware counters located within the performance monitoring unit;

wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type.

2. (Original) The system of claim 1, wherein the one or more hardware counters count the occurrence of events during a state of the interrupt of the selected type.

3. (Currently amended) The system of claim 2, wherein states of the interrupt include interrupt on, interrupt taken and interrupt acknowledged ~~accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return~~.

4. (Currently amended) The system of claim 1, wherein multiple types of events are counted during the processing of the interrupt.

5. (Currently amended) The system of claim 1, wherein the one or more hardware counters count the occurrence of events according to the type of interrupt during which [[they]] the events occur.

6. (Original) The system of claim 1, wherein the events include clock cycles and cache misses.

7. (Currently amended) The system of claim 1, wherein a second interrupt interrupts ~~a first~~ the interrupt of the selected type, and wherein the hardware counters count events separately that occur during the processing of the interrupt of the selected type ~~first~~ and during processing of the second interrupt ~~interrupts~~.

8. (Currently amended) A method of executing instructions on an information processing system, comprising the steps of:

receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

counting at least one event for a selected state of the plurality of states [[for]] during processing of the interrupt.

9. (Currently amended) The method of claim 8, wherein the step of counting includes counting at least one event for each of the plurality of states during the processing of the interrupt.

10. (Currently amended) The method of claim 8, wherein the plurality of states include interrupt on, interrupt taken and interrupt acknowledged ~~accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return~~.

11. (Original) The method of claim 8, wherein the at least one event includes clock cycles and cache misses.

12. (Currently amended) The method of claim 8, wherein the step of counting includes counting multiple types of events for the same state during the processing of the interrupt.

13. (Currently amended) The method of claim 8, wherein the step of counting is performed by one or more hardware counters during the processing of the interrupt.

14. (Currently amended) The method of claim 8, wherein the events are counted according to the type of interrupt during which [[they]] the events occur.

15. (Currently amended) The method of claim 8, wherein ~~a first~~ the interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the processing of the interrupt ~~the first~~ and during processing of the second interrupt ~~interrupts~~.

16. (Currently amended) A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions for receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

second instructions for counting at least one event for a selected state of the plurality of states [[for]] during processing of the interrupt.

17. (Currently amended) The computer program product of claim 16, wherein the plurality of states include interrupt on, interrupt taken and interrupt acknowledged ~~accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return~~.

18. (Previously presented) The computer program product of claim 16, wherein the at least one event includes clock cycles and cache misses.

19. (Currently amended) The computer program product of claim 16, wherein the second instructions for counting count multiple types of events for the same state [[of]] during the processing of the interrupt.

20. (Currently amended) The computer program product of claim 16, wherein the step of counting is performed by one or more hardware counters during the processing of the interrupt.

21. (Currently amended) The computer program product of claim 16, wherein the events are counted according to the type of interrupt during which [[they]] the events occur.

22. (Currently amended) The computer program product of claim 16, wherein ~~a first~~ the interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the processing of the interrupt and during processing of the ~~first and~~ second interrupt ~~interrupts~~.